CLAIMS

1. A method for performing static timing analysis of a digital system in the presence of a plurality of global sources of delay variation comprising the steps of:

a) selecting, for at least one timing test, at least one pair of an early path and a late path leading to said timing test;

b) identifying at least one global parameter which the delays of said early and late paths depend on;

c) determining for at least one of said global parameters at least one consistent value assignment; and

d) computing for each said consistent assignment a slack value for said path pair.

2. The method as recited in claim 1 wherein one of said early and late paths is a clock path and the other of said early and late paths is a data path.

3. The method as recited in claim 1, wherein said at least one timing test comprises those timing tests within said digital system whose slack falls below a specified threshold after an initial static timing analysis.

4. The method as recited in claim 1, wherein said identified path pair comprises a late critical path to said timing test and an early critical path to said timing test.

5. The method as recited in claim 1, wherein said initial static timing analysis is performed using bounding parameter values.

6. The method as recited in claim 1, further comprising the step of determining for each of said timing tests the worst of said computed slacks.

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7. The method as recited in claim 1, wherein said step c) further comprises the steps of:

e) enumerating combinations of realizable values of at least one of said identified parameters; and

f) performing a timing analysis for each of said enumerated combinations.

8. The method as recited in claim 7, wherein said step e) is terminated after one of the timing analyses of step f) produces a slack below a specified threshold.

9. The method as recited in claim 7, wherein at least one parameter whose realizable values are enumerated comprises a subset of the parameters identified in step b).

10. The method as recited in claim 9, wherein said step e) is repeatedly applied to additional ones of said identified parameters until said step f) results in a slack which is greater than a specified slack threshold.

11. The method as recited in claim 1, wherein said step b) further comprises identifying parameters in which delay functions are separable, and said step c) further comprises setting independently each of said parameters in which delay functions are separable to the value that results in the worst slack value at said timing test.

12. The method as recited in claim 11, wherein said step of independently setting parameter values further comprises the steps of:

e) summing along the early and late paths of said path pair sensitivities of delay elements with respect to each of said parameters in which delay functions are separable;

f) computing the difference between said summed path sensitivities of said early and late paths, and

g) determining a value of each of said parameters in which delay functions are separable according to an arithmetic sign of said difference of sensitivities.

13. The method as recited in claim 6, further comprising the step of determining whether the slack of any other early and late path pair to said timing test is worse than said determined worst slack, and if so, repeating said steps b), c), and d) for said other path pair.

14. The method as recited in claim 1, wherein the timing analysis is performed at a gate-level.

15. The method as recited in claim 1, wherein the timing analysis is performed at a transistor-level.

16. The method as recited in claim 1, wherein the delay models are stored as pre-determined tables.

17. The method as recited in claim 1, wherein the delay models are stored as pre-determined analytic equations.

18. The method as recited in claim 1, wherein the delay models are computed on the fly.

19. The method as recited in claim 1, wherein the circuit comprises a plurality of clock domains.

20. The method as recited in claim 1, wherein the circuit is selected from the group consisting of at least one of the following clock configurations: mesh network, tree network, hybrid network, gated clocks and pulsed clocks.

21. The method as recited in claim 1, wherein the sources of variability include a mistrack between one or more of the following device families that is selected from the

group consisting of devices having different threshold voltages, devices having different gate oxide thicknesses and devices having different characteristics for PFET and NFET devices.

22. The method as recited in claim 1, wherein the sequential elements are selected from the group consisting of at least one of: master-slave latches, flip-flops, edge-triggered latches, level-sensitive latches and transparent latches.

23. The method as recited in claim 1, wherein the timing analysis is conducted for timing verification at one or more levels selected from the group consisting of a circuit level, macro level, functional-unit level, chip level, board level and system level.

24. The method as recited in claim 1, wherein the circuit being analyzed is selected from the group consisting of at least one of the following technologies: CMOS, domino, static logic and dynamic logic.

25. The method as recited in claim 1, wherein the global sources of variation include one or more of manufacturing variations, device fatigue variations, environmental variations, modeling variations, and circuit operation variations.

26. A system for performing static timing analysis of a digital system in the presence of a plurality of global sources of delay variation comprising:

a) means for selecting, for at least one timing test, at least one pair of an early path and a late path leading to said timing test;

b) means for identifying at least one global parameter which the delays of said early and late paths depend on;

c) means for determining for at least one of said global parameters at least one consistent value assignment; and

d) means for computing for each said consistent assignment a slack value for said path pair.

27. The system as recited in claim 26, wherein element c) further comprises:

e) means for enumerating combinations of realizable values of at least one of said identified parameters; and

f) means for performing a timing analysis for each of said enumerated combinations.

28. The system as recited in claim 26, wherein said element b) further comprises means for identifying parameters in which delay functions are separable, and said element c) further comprises means for setting independently each of said parameters in which delay functions are separable to the value that results in the worst slack value at said timing test.

29. The system as recited as recited in claim 28, wherein said means of independently setting parameter values further comprises:

e) means for summing along the early and late paths of said path pair sensitivities of delay elements with respect to each of said parameters in which delay functions are separable;

f) means for computing the difference between said summed path sensitivities of said early and late paths, and

g) means for determining a value of each of said parameters in which delay functions are separable according to an arithmetic sign of said difference of sensitivities.

30. A program storage device readable by a machine, tangibly, embodying a program of instructions executable by the machine to perform method steps for performing static

timing analysis of a digital system in the presence of a plurality of global sources of delay variation, said method steps comprising:

a) selecting, for at least one timing test, at least one pair of an early path and a late path leading to said timing test;

b) identifying at least one global parameter which the delays of said early and late paths depend on;

c) determining for at least one of said global parameters at least one consistent value assignment; and

d) computing for each said consistent assignment a slack value for said path pair.

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